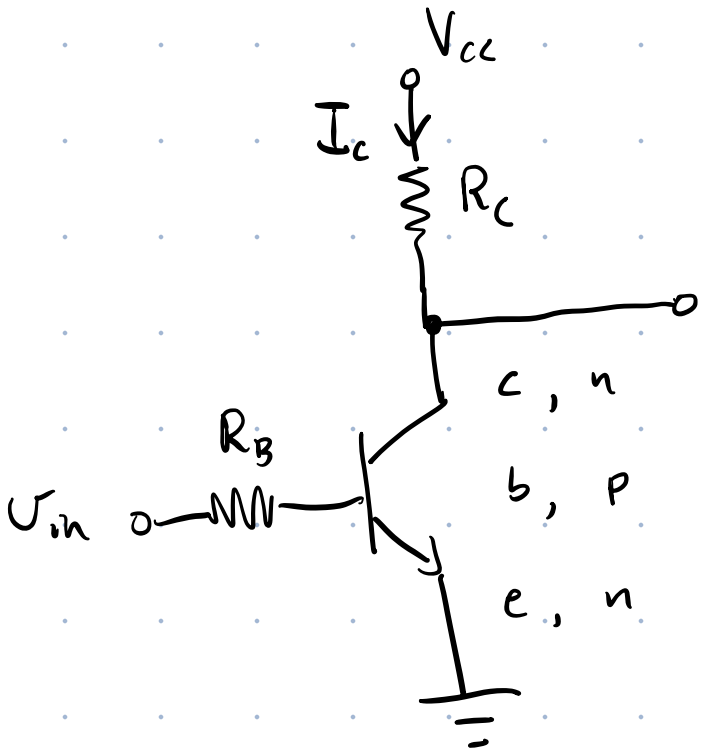
PHYS 231 Dec. 2, 2024

Last Week:

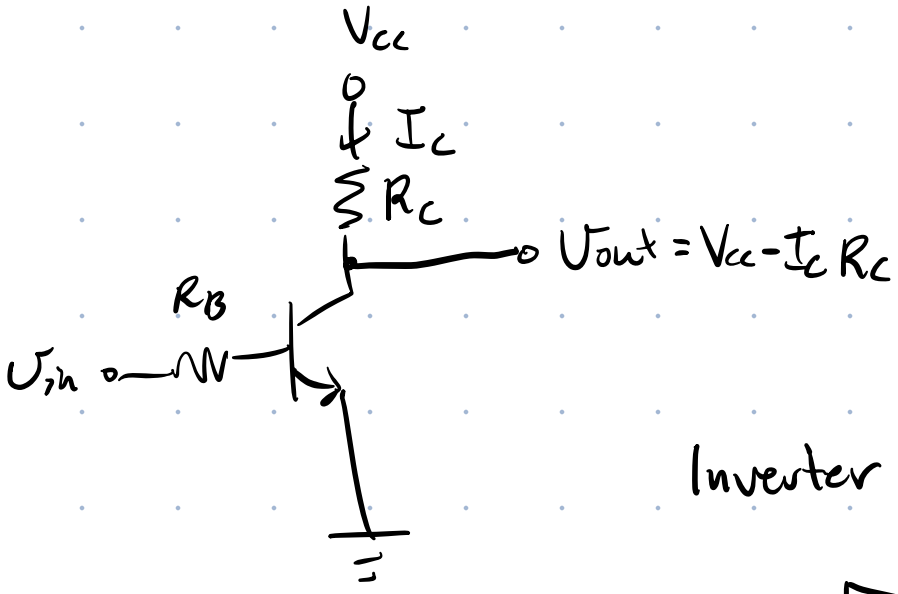
Transistor Switch



If V_{in} is LO, $I_c = 0$

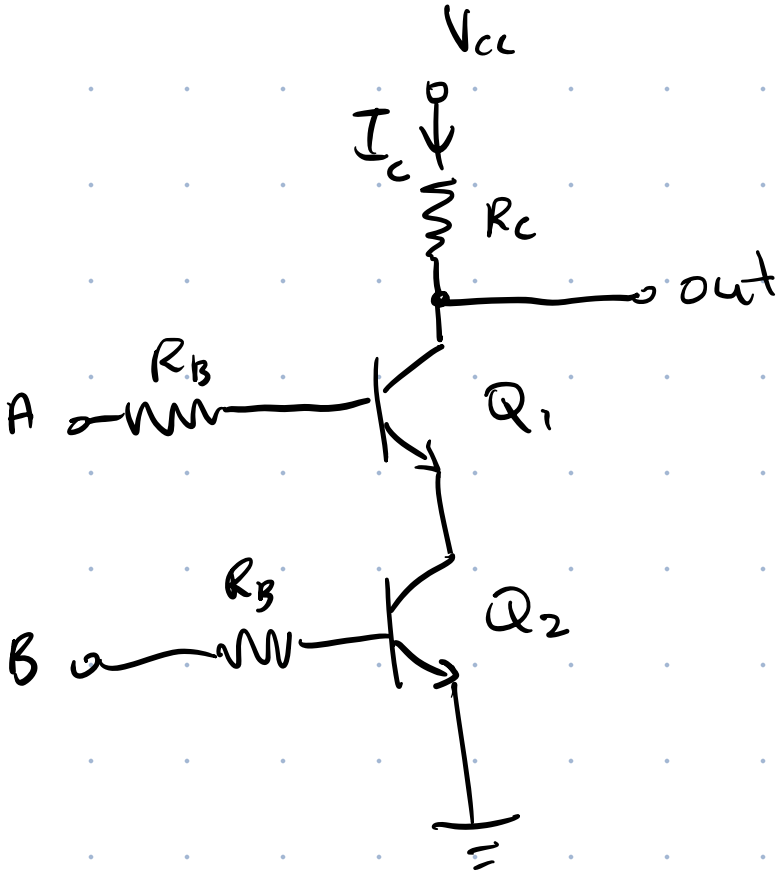
If V_{in} is HI, $I_c \neq 0$

} transistor acts as an electronic switch. The voltage at the base controls the current through the transistor



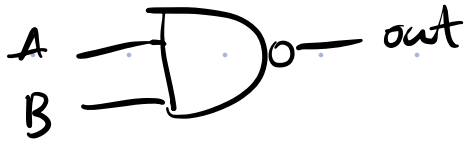
V_{in}	V_{out}
0	1
1	0

Inverter (NOT gate)

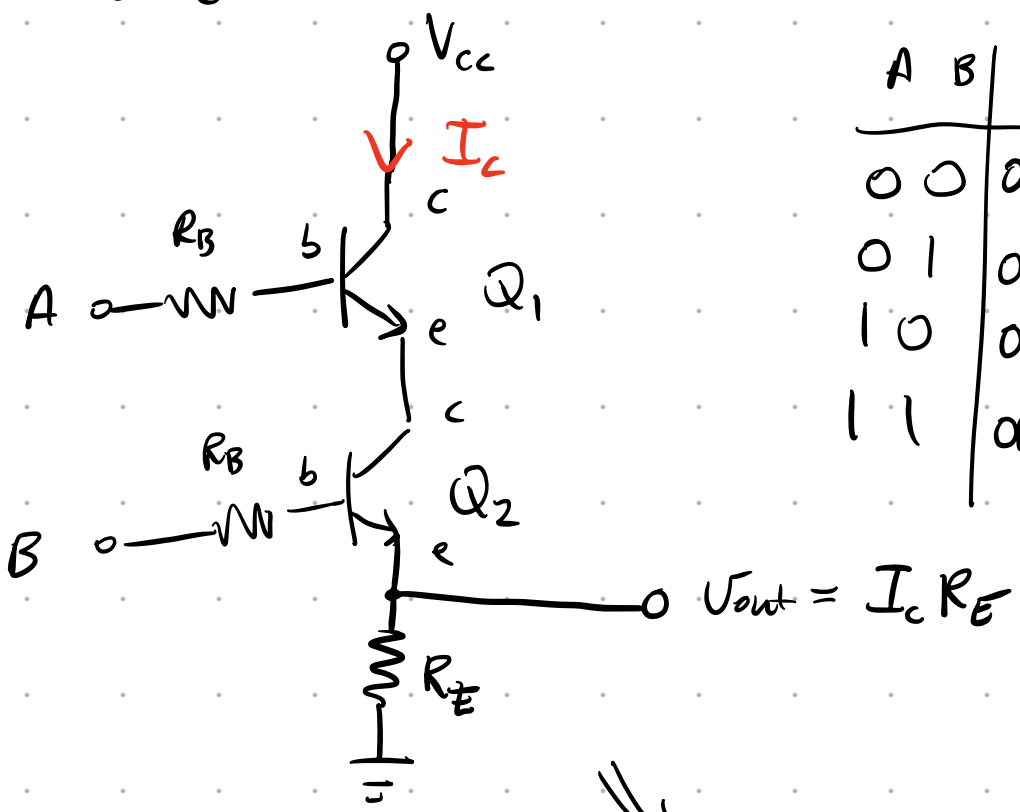


A	B	Q_1	Q_2	I_c	out
0	0	OFF	OFF	0	1
0	1	OFF	ON	0	1
1	0	ON	OFF	0	1
1	1	ON	ON	≠0	0

NAND gate



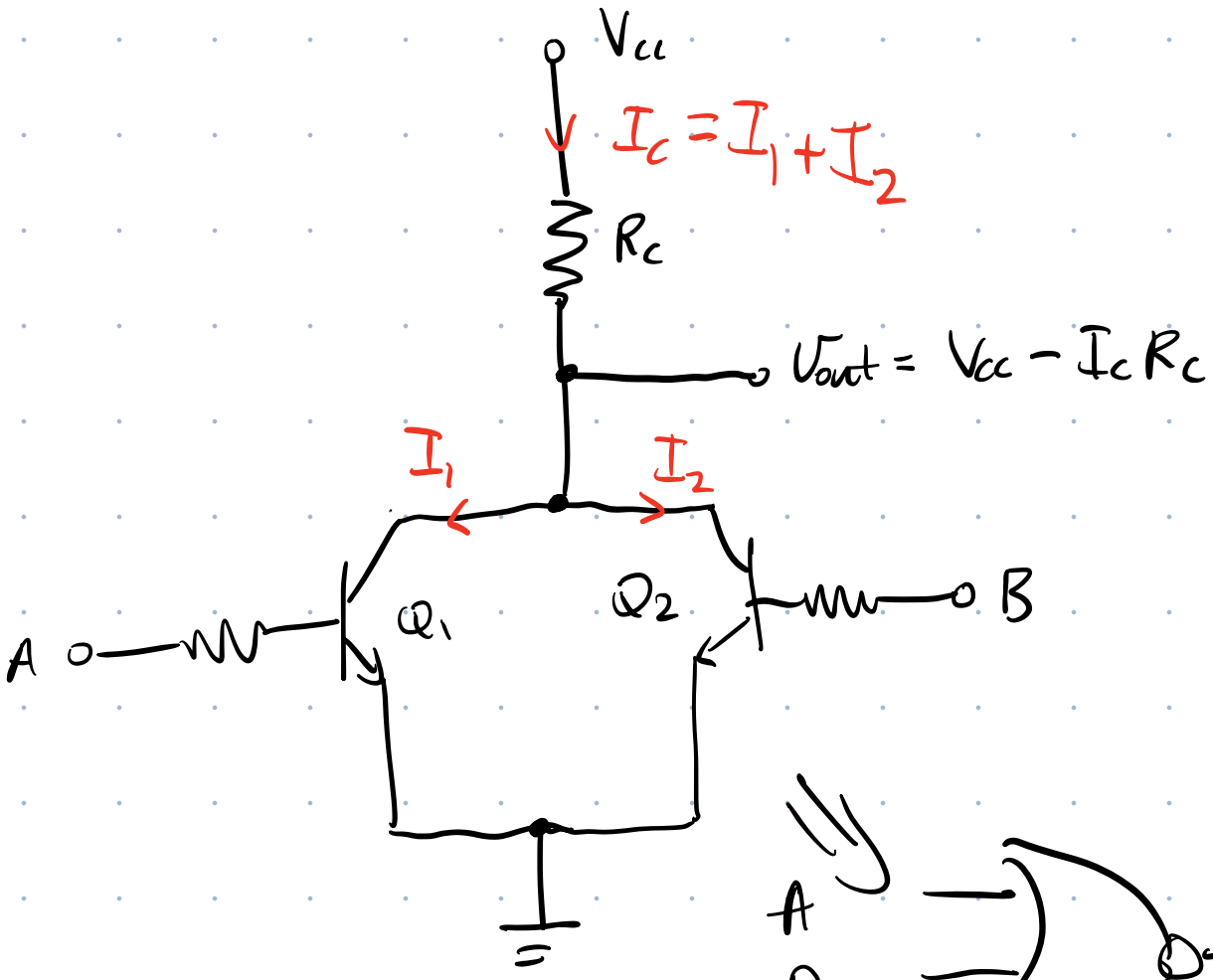
To make an AND gate, consider moving the output to R_C.

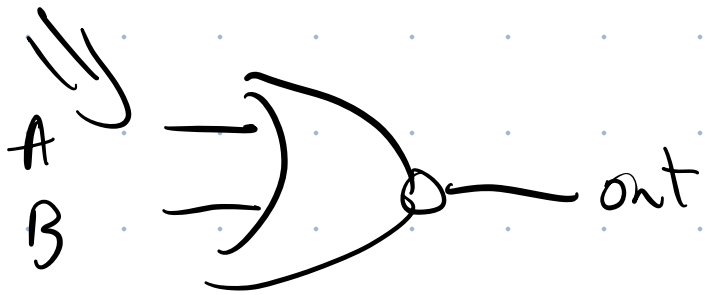


A	B	Q_1	Q_2	I_C	V_{out}
0	0	OFF	OFF	0	0
0	1	OFF	ON	0	0
1	0	ON	OFF	0	0
1	1	ON	ON	$\neq 0$	1

AND truth table

Let's try a parallel combination of transistors.



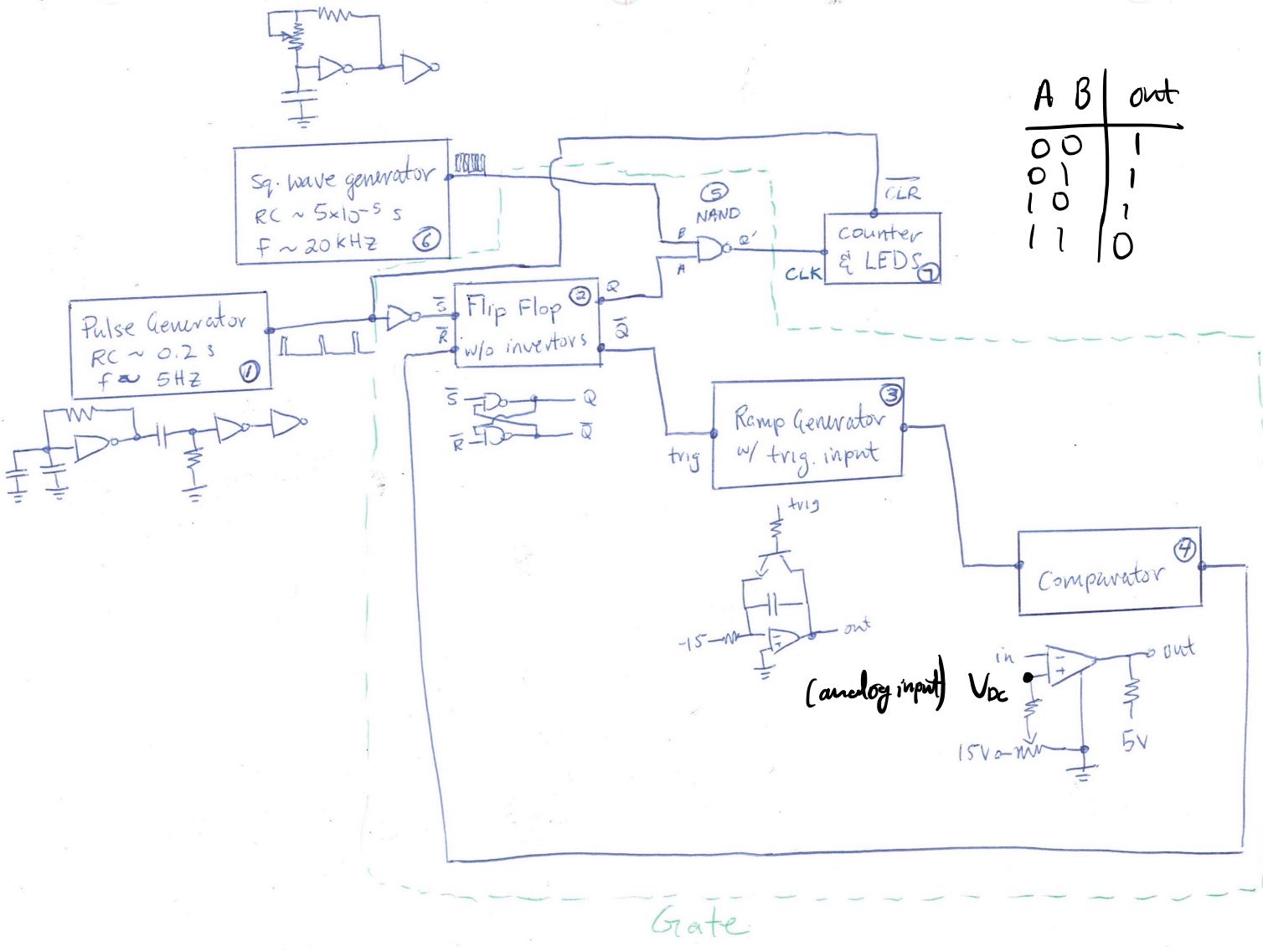


Truth table

A	B	Q_1	Q_2	I_c	V_{out}
0	0	OFF	OFF	0	1
0	1	OFF	ON	$\neq 0$	0
1	0	ON	OFF	$\neq 0$	0
1	1	ON	ON	$\neq 0$	0

NOR

ADC Block Diagram



A	B	out
0	0	1
0	1	1
1	0	1
1	1	0

Goal of ADC is to output a binary (digital) representation of an analog DC voltage.

If the V_{DC} is 5.3 V, want the output to look like:

5	3
0101	0011

Need 53 clock pulse passed to the counter. Once reach desired no. of counts, block further clock pulse from reaching the counter so that we can read a stable output. Keep this stable output until a reset pulse clears the counter. Then, initiate the counting again.

① Assume that counter just cleared by a reset pulse.

② $\overline{S}$ is HI, but was just pulsed LO $\Rightarrow Q=1, \overline{Q}=0$

③ Since $\overline{Q}=0$, transistor is <u>not</u> conducting $\{$ the ramp generator is producing a ramp.

④ Initially, ramp input is less than V_{DC}. $\therefore$ comparator output is HI.

⑤ Sq. wave gen. continuously output square waves.

Initially, since $Q=1$, the NAND gate ⑤ passes clock pulse to the counter $\{$ the counter is actively counting.

(4) Eventually, the ramp output reaches V_{DC} which causes the comparator output Hi → LO.

(2) LO comparator output ($\overline{R}$) causes flip flop to change state $(Q, \overline{Q}) = (1,0) \rightarrow (0,1)$.

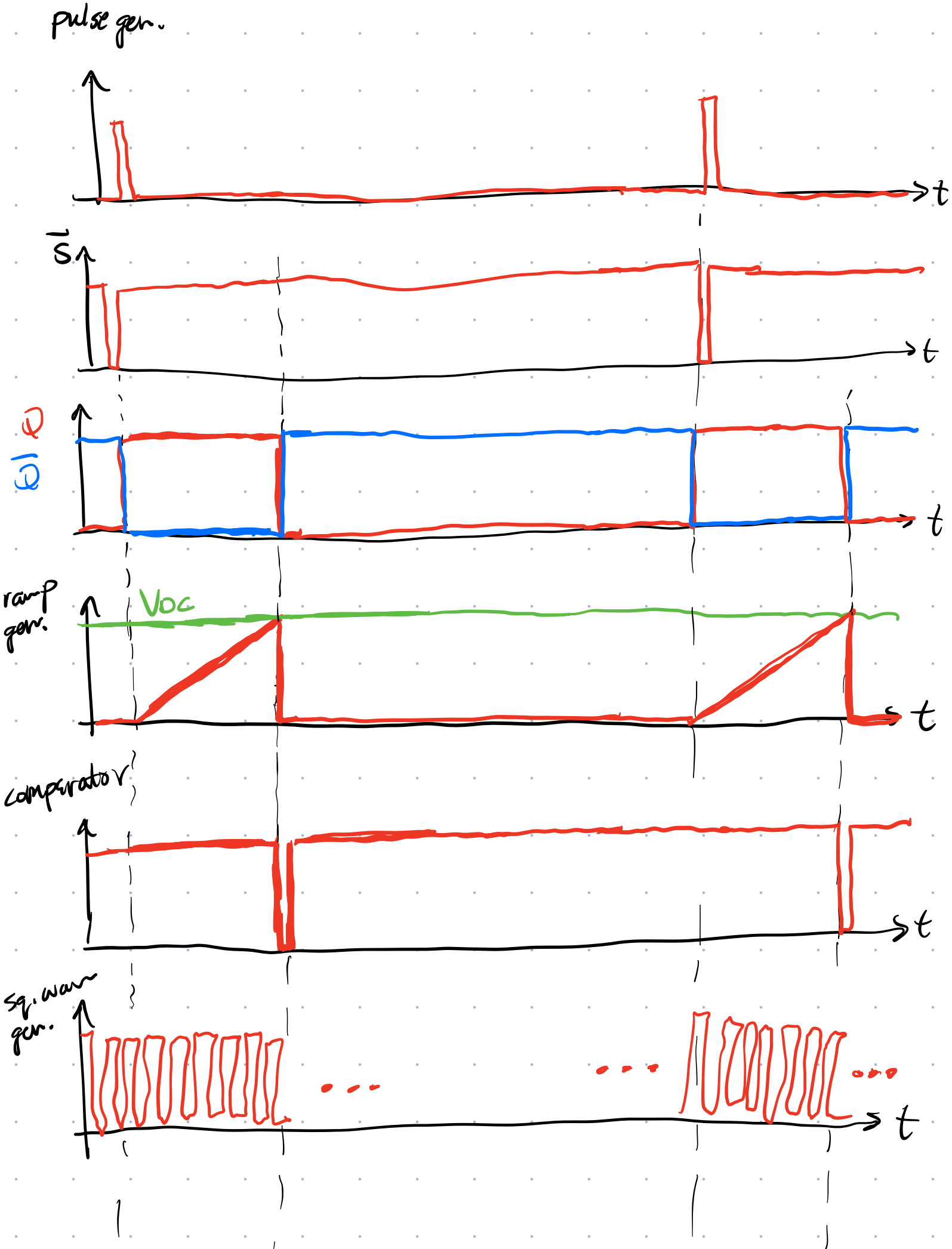
Now, with $Q = 0$, the output of NAND gate is always Hi. ∴ no clock pulse reach the counter & its output is stable.

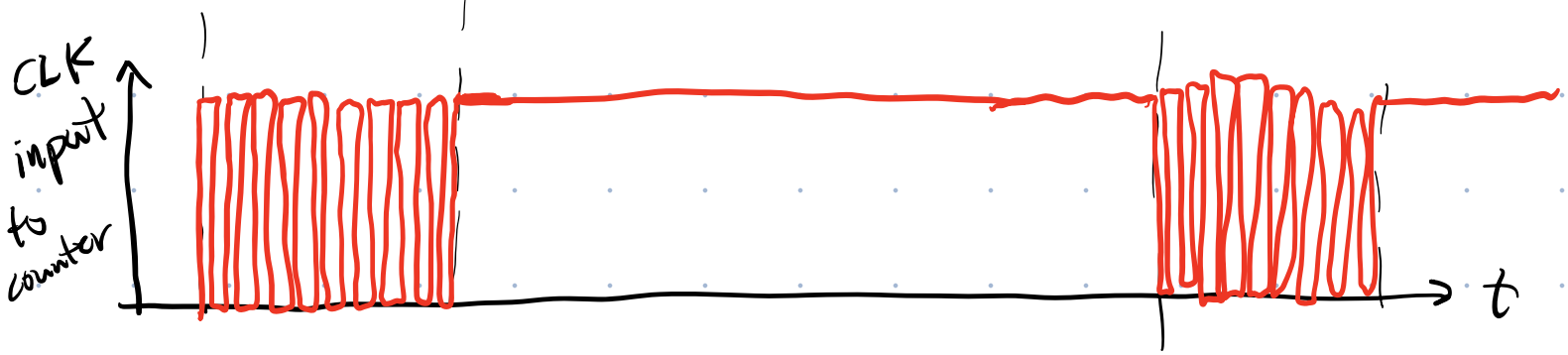
(3) Now $\overline{Q} = 1$ which makes transistor conducting s.t. ramp generator output is zero.

(4) Since ramp is zero, compartor output is Hi again.

(5) Since Q = LO, output of NAND is always Hi.
∴ Clock pulses <u>not</u> passed to counter & counter output is stable.

This remains the case unit the next reset pulse arrives & the entire sequence repeats.


pulse gen.
t
$\bar{S}$
t
Q
$\bar{Q}$
t
ramp gen.
Voc
t
comparator
t
sq. wave gen.
t


CLK
input
to
counter
t