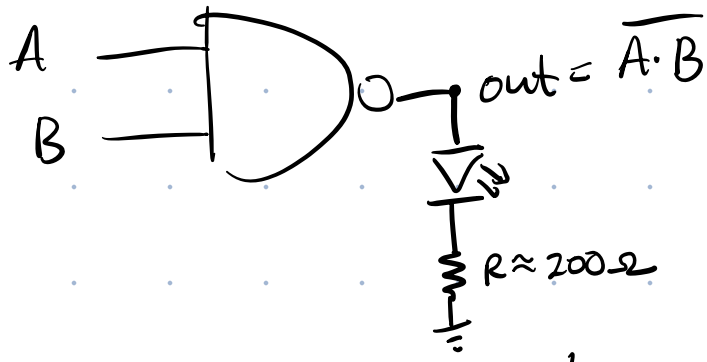
PHYS 231 Nov. 6, 2024

Last Time:

Logic Gates & Truth tables.

Eg NAND gate



A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Today: Flip-Flop & Binary Nos.

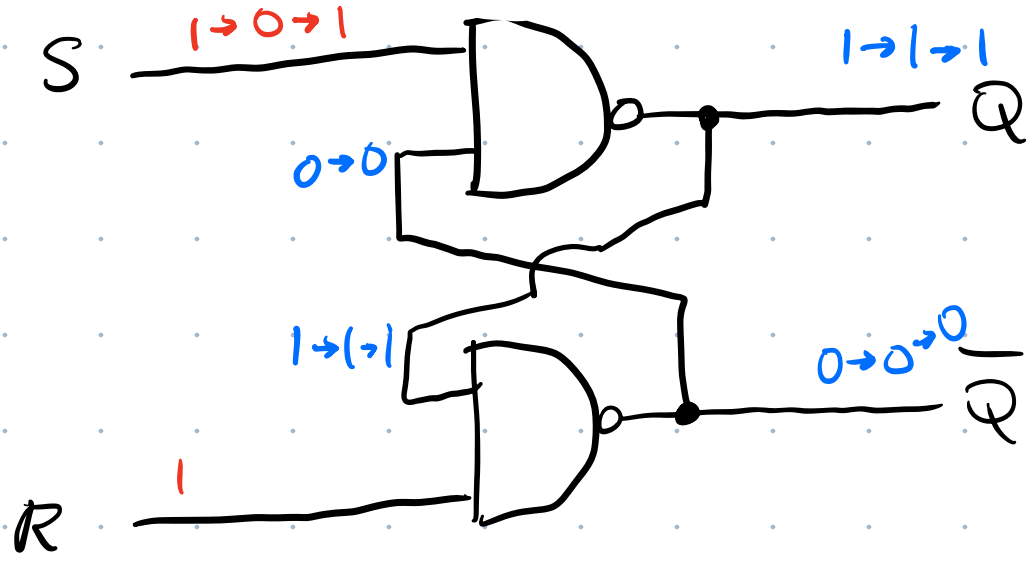
So far, all logic gate outputs depend on instantaneous states of inputs. Want to design a device that has some memory capability.

R-S Flip Flop

reset set.

The R-S Flip-Flop is a two-input device (R & S) with two outputs. State of outputs $(Q, \bar{Q})$ tells the user which of R or S was the last to be LO. That is, the flip flop "remembers" which of the two inputs was last to be LO.

R-S Flip Flop.



NAND truth table

0 0	1
0 1	1
1 0	1
1 1	0

What are the possible outputs $(Q, \bar{Q})$?

$(Q, \bar{Q}) = \cancel{(0,0)}$, $(0,1)$ ✓, $(1,0)$ ✓, $\cancel{(1,1)}$

Take $(S, R) = (1, 1)$ (i.e. both inputs HI) as the default state for inputs.

Cannot have $(Q, \bar{Q}) = (0, 0)$ when $(S, R) = (1, 1)$

" " " $= (1, 1)$ " " " "

When $(S, R) = (1, 1)$, output of flip flop has two possible stable states. $\Rightarrow$ output is bistable.

What happens if one of S or R momentarily drops to LO?

Case 1: Initial

$S = 1$	$R = 1$	$Q = 0$	$\bar{Q} = 1$
↓	↓	↓	↓
0	1	1	0
↓	↓	↓	↓
1	1	1	0

When S is Last to be LO, $(Q, \bar{Q}) = (1, 0)$.

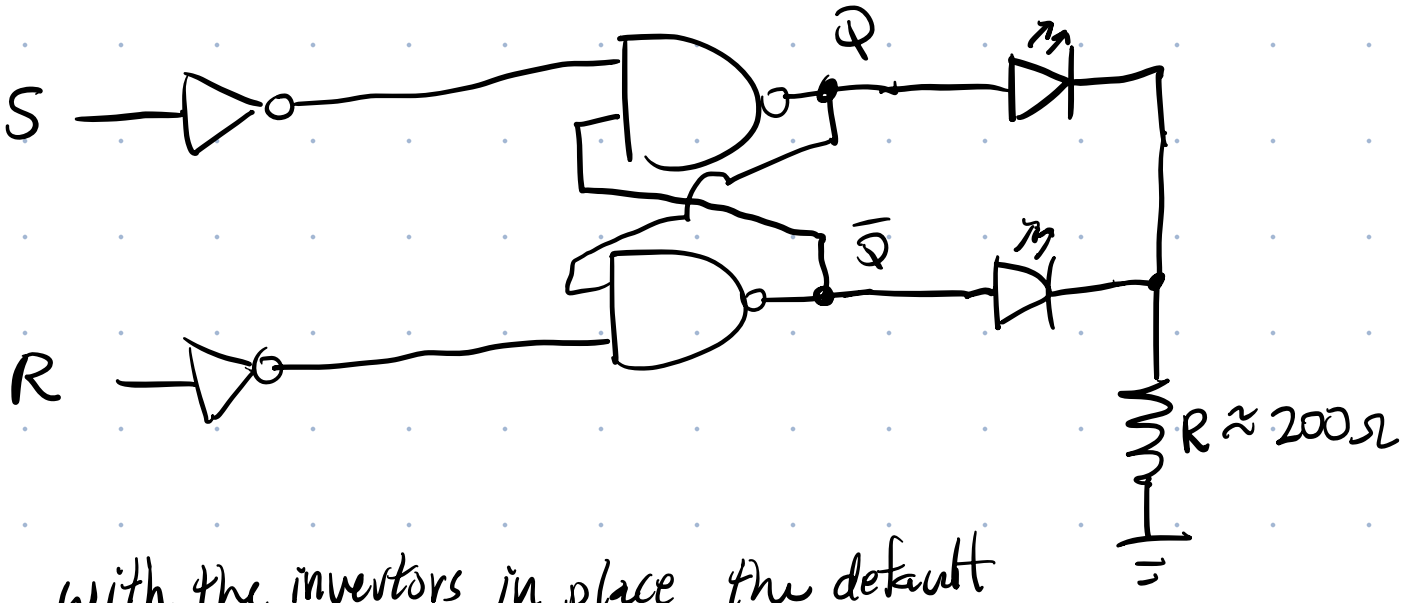
Case 2: Initial

$S = 1$	$R = 1$	$Q = 1$	$\bar{Q} = 0$
↓	↓	↓	↓
0	1	1	0
↓	↓	↓	↓
1	1	1	0

It is still the case that, when S is Last to be LO, $(Q, \bar{Q}) = (1, 0)$.

Exercise for the student: Show that, regardless of the initial state of $(Q, \bar{Q})$, allowing R to go LO temporarily "resets" the output to $(Q, \bar{Q}) = (0, 1)$.

Circuit you will build in Lab #7 is



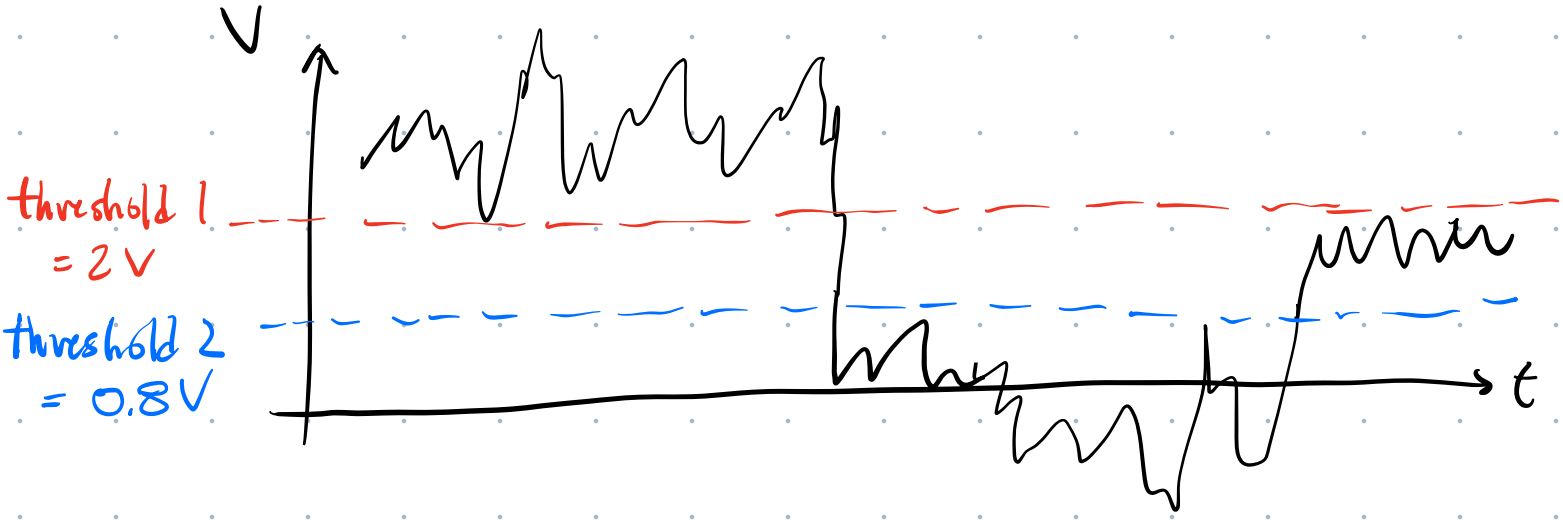
with the inverters in place, the default state of the input is $(S, R) = (0, 0)$.

Output is determined by which of S or R was last Hi.

If S last Hi, $(Q, \bar{Q}) = (1, 0)$
If R last Hi, $(Q, \bar{Q}) = (0, 1)$

Digital Electronics

Consider the following noisy signal



Voltage signal w/ large fluctuations.

- In digital electronics, define a HI (1) as anything greater than threshold 1.
- Define LO (0) as anything below threshold 2.
- Signals between thresholds 1 & 2 are undefined.

⇒ we get some noise immunity by defining our thresholds for LO & HI signals.

⇒ stable digital signals even w/ large volt. fluc.

Binary Nos.

Only 2 digits: 0, 1 (base 2)

Decimal system (base 10) → 10 digits (0, 1, 2, ... 9)

Can represent any base 10 no. in the following way:

$$153_{10} = 1 \cdot 10^2 + 5 \cdot 10^1 + 3 \cdot 10^0$$

base 10

In the same way, we can express binary nos as.

$$10110 = 1 \cdot 2^4 + 0 \cdot 2^3 + 1 \cdot 2^2 + 1 \cdot 2^1 + 0 \cdot 2^0$$

$2^4\ 2^3\ 2^2\ 2^1\ 2^0$

$$= 16 + 0 + 4 + 2 + 0$$

$$= 22$$

$$10110_2 = 22_{10}$$

Note that $153_{10} = \underbrace{10011001}_{\text{8-bit binary no.}}{}_2$

First 10 binary nos.

0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9